PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-335173
(43)Date of publication of application : 17.12.1993

(51)Int.CI. H01G 4/12
H01G 4/12
H01G 4/12

(21)Application number : 04-164181
(22)Date of filing : 28.05.1992

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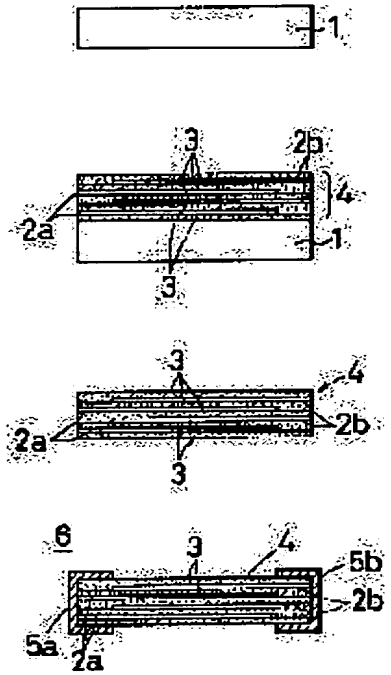
(54) LAMINATED CERAMIC ELECTRONIC COMPONENT AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To realize a laminated ceramic electronic component lessened in thickness and enhanced in performance.
CONSTITUTION: A ceramic-metal laminate 4 composed of conductor electrodes 2a and 2b formed through a CVD method, an evaporation method, or a sputtering method and ceramic layers 3 laminated through a CVD method is provided onto an Al2O3 substrate 1. Thereafter, the Al2O3 substrate 1 is selectively removed through a dry etching method or the like to leave only the ceramic- metal laminate 4. In succession, outer electrodes 5a and 5b are formed on both the ends of the laminate 4 through dipping, and thus a small laminated ceramic capacitor 6 is obtained.



LEGAL STATUS

[Date of request for examination] 26.05.1999
[Date of sending the examiner's decision of rejection] 27.02.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of

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CLAIMS

[Claim(s)]
[Claim 1] Laminating ceramic electronic parts characterized by carrying out the laminating of the conductor electrode of two or more layers, and the two or more layers ceramic layer formed by the CVD method by turns.
[Claim 2] Laminating ceramic electronic parts according to claim 1 which formed said conductor electrode using a CVD method, vacuum deposition, or at least one sort of approaches of the spatters.
[Claim 3] The manufacture approach of the laminating ceramic electronic parts characterized by removing said substrate after carrying out two or more layer laminating of a conductor electrode and the ceramic layer by the CVD method by turns on a substrate.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to laminating ceramic electronic parts and its manufacture approach. Speaking concretely, being related with laminating ceramic electronic parts and its manufacture approaches, such as a stacked type ceramic condenser widely used for electronic parts, such as a video tape recorder, a laminating varistor, a laminating piezoelectric device, and a multilayered ceramic substrate.
[0002]
[Description of the Prior Art] The manufacture approach of the conventional stacked type ceramic condenser is explained (not shown). First, after printing electrode paste (internal electrode), such as a silver system paste, and making it dry on the ceramic student sheet cut into bigger predetermined magnitude than a component dimension, two or more ceramic student sheets with which this electrode paste was printed are made to stick by pressure in piles. Subsequently, this is cut into the magnitude of one element and calcinated. After baking, as it is made to flow with an internal electrode, electrode paste is applied on the surface of a component, this can be burned, an external electrode is formed in the both ends of a component, and the chip-like stacked type ceramic condenser is manufactured.
[0003]
[Problem(s) to be Solved by the Invention] In recent years, in the field of electronic parts, much more micrifying and high-performance-izing of a stacked type ceramic condenser etc. of electronic parts are desired with the densification and high integration of an electronic circuitry. Therefore, in a stacked type ceramic condenser, in order to micrify without making capacity small, to make thickness of a ceramic layer (dielectric layer) as thin as possible is desired.
[0004] However, when it was going to make thickness of a ceramic layer thin in a laminating ceramic condenser like before, there were various problems. First, although it is necessary to make small ceramic raw material powder particle size in order to make a ceramic layer thin, there is a limit in micrifying of the particle size of ceramic raw material powder. Moreover, if a ceramic layer is made thin, since the thickness of an internal electrode is also thin and it is necessary to carry out, in a baking process, it is easy to produce an electrode piece in an internal electrode. Furthermore, if a ceramic layer is made thin, short-circuit will occur with abnormality growth of the internal electrode at the time of baking, or the problem of pressure-proofing falling with the hole generated in the ceramic layer will arise. For this reason, if it was in the conventional stacked type ceramic condenser, it was impossible to have made thickness of a ceramic layer thinner than several micrometers, and there was a limitation in micrifying and large-capacity-izing of a stacked type ceramic condenser.
[0005] The place which this invention is made in view of the fault of the above-stated conventional example, and is made into the purpose is to carry out lamination of the ceramic layer, realizing high performance of laminating ceramic electronic parts.
[0006]
[Means for Solving the Problem] The laminating ceramic electronic parts by this invention are characterized by carrying out the laminating of the conductor electrode of two or more layers, and the two or more layers ceramic layer formed by the CVD method by turns.
[0007] Furthermore, the above-mentioned conductor electrode can be formed using a CVD method, vacuum deposition, or at least one sort of approaches of the spatters.

[0008] Moreover, after the manufacture approach of the laminating ceramic electronic parts by this invention carries out two or more layer laminating of a conductor electrode and the ceramic layer by the CVD method by turns on a substrate, it is characterized by removing said substrate.
[0009]
[Function] If it is in the laminating ceramic electronic parts of this invention, since a ceramic layer is formed by the CVD method and the conductor electrode is further formed of a CVD method, vacuum deposition, a spatter, etc., the film with both a ceramic layer and a precise conductor electrode is formed, moreover, since it does not pass through heating processes, such as baking, it is hard to produce defects, such as an electrode piece of a conductor electrode, and short-circuit, and high performance-ization as electronic parts is attained.
[0010] Furthermore, since a ceramic layer is formed by the CVD method and the conductor electrode is formed of a CVD method, vacuum deposition, a spatter, etc., the lamination 1 micrometer or less of a ceramic layer or a conductor electrode becomes possible, and micro laminating ceramic electronic parts are obtained.
[0011] Moreover, if it is in the manufacture approach of the laminating ceramic electronic parts of this invention, since the ceramic layer and the conductor electrode are formed on a substrate, a ceramic layer ultra-thin as a base material and a conductor electrode can be grown up, and the laminating of the substrate can be carried out by turns. And since the substrate is finally removed, laminating ceramic electronic parts do not become large with a substrate, and the above micro laminating ceramic electronic parts can be manufactured.
[0012]
[Example] Drawing 1 (a), (b), (c), and (d) show the manufacture approach of the stacked type ceramic condenser by one example of this invention. A front face is the smooth substrate 1 and what is shown in drawing 1 (a) is not limited to an insulating substrate by etching etc. that what is necessary is just the removable quality of the material alternatively. For example, an alumina substrate etc. can be used. As shown on this substrate 1 at drawing 1 (b), the ceramic layer 3 is formed, conductor electrode 2a of the 1st layer is formed on it, the ceramic layer 3 is formed on it, conductor electrode 2b of a two-layer eye is formed further, the ceramic layer 3 is formed further, and conductor electrode 2a of the 3rd layer is formed on it. By repeating such a process, the laminating of conductor electrode 2a, 2b, and every two or more layers of the ceramic layers 3 is carried out to the front face of a substrate 1 by turns, and the ceramic-metal layered product 4 which consists of two or more layers conductor electrode 2a, 2b, and the two or more layers ceramic layer 3 is formed. Here, each ceramic layer 3 is formed by the CVD method, each conductor electrode 2a and 2b are formed using one of approaches among a CVD method, vacuum deposition, or a spatter, and thickness of each ceramic layer 3 and each conductor electrode 2a, and 2b is set to 1 micrometer or less. Moreover, conductor electrode 2a used as an internal electrode and 2b are patternized using the mask, and conductor electrode 2a of the oddth layer and conductor electrode 2b of the eventh layer are pulled out by turns to the edge of the opposite side. Then, if etching etc. removes a substrate 1 alternatively, only the ceramic-metal layered product 4 as shown in drawing 1 (c) will remain. Subsequently, if the external electrodes 5a and 5b are formed in both ends by dipping, a spatter, etc., conductor electrode 2a of the oddth layer will flow with one external electrode 5a, conductor electrode 2b of the eventh layer will flow with external electrode 5b of another side, and the micro laminating ceramic condenser 6 as shown in drawing 1 (d) will be manufactured.
[0013] In addition, although drawing 1 explains one production process, a laminating ceramic condenser can be efficiently manufactured by manufacturing two or more elements to coincidence.
[0014] Below, a concrete example is hung up and explained in order to explain this invention more clearly. Example 1 drawing 2 is the outline block diagram of heat CVD system 7 used for manufacture of a stacked type ceramic condenser 6. A susceptor for the chamber for CVD in 8 and 9 to set a substrate 1, The feed way of 10O2 gas and 11 the feed way of Ar carrier gas, and 12 The bessel of TIP [titanium isopropoxide], The bessel of Pb (C2H5)4 and 14 13 The bessel of La (DPM) [DPM=C11H19O2]3, 15 is the bessel of 2(PtCl2) (CO) 3, and each bessels 12, 13, 14, and 15 of TIP, Pb (C2H5)4, La (DPM)3, and (PtCl2) 2(CO) 3 are arranged on the feed way 11 of Ar carrier gas at juxtaposition.
[0015] This 2Oaluminum3 substrate 1 was set on the susceptor 9 of heat CVD system 7, using 50mm each of every direction, and 2Oaluminum3 substrate with a thickness of 0.2mm as a substrate 1 for manufacturing a stacked type ceramic condenser 6.
[0016] Subsequently, where a susceptor 9 is heated at 600 degrees C, each bulbs 16, 17, and 18 of each bessels 12, 13, and 14 of TIP, Pb (C2H5)4, and La (DPM)3 are opened. Each material gas of TIP, Pb (C2H5)4, and La

(DPM)3 which were evaporated is put on Ar carrier gas. To a chamber 8 Delivery, This material gas was made to spray and react to 2Oaluminum3 substrate 1 with O2 gas, and the PLT thin film 21 (ceramic layer 3) with a thickness of about 1 micrometer was formed (henceforth a PLT film formation process).

[0017] Next, set a metal mask on the PLT thin film 21, and where a substrate 1 is heated at 600 degrees C, the bulb 19 of the bessel 15 of 2(PtCl2) (CO) 3 is opened. (PtCl2) 2 (CO) The material gas of 3 is sprayed on aluminum2O3 substrate 1 through the aperture of a metal mask with Ar carrier gas. As shown in drawing 3 (a) and (b), with a thickness of about 0.5 micrometers Pt film 20a (conductor electrode 2a) was formed in the same pattern as the aperture of a metal mask (henceforth the 1st process of Pt film formation). Drawing 3 (b) is the X section enlarged drawing of drawing 3 (a), the field which gave the slash shows the field equivalent to one element, and the figure written down in drawing 3 (b) shows the dimension (unit mm) of each part.

[0018] Subsequently, the PLT film formation process was made to generate about 1 micrometer of PLT thin films 21 again.

[0019] Next, another metal mask is set on the PLT thin film 21 of the maximum upper layer. Where a substrate 1 is heated at 600 degrees C, the bulb 19 of the chamber 15 of 2(PtCl2) (CO) 3 is opened. (PtCl2) 2 (CO) The material gas of 3 is sprayed on aluminum2O3 substrate 1 through the aperture of a metal mask with Ar carrier gas. As shown in drawing 4 (a) and (b), with a thickness of about 0.5 micrometers Pt film 20b (conductor electrode 2b) was formed in the same pattern as the aperture of a metal mask (henceforth the 2nd process of Pt film formation). Drawing 4 (b) is the Y section enlarged drawing of drawing 4 (a), the field which gave the slash shows the field equivalent to one element, and the figure written down in drawing 3 (b) shows the dimension (unit mm).

[0020] the [thus, / PLT thin film formation-Pt film formation] -- each process of the 1-PLT thin film formation-Pt film formation 2nd was repeated 150 times, finally the PLT film formation process was performed, and the ceramic-metal layered product 4 was obtained on 2Oaluminum3 substrate 1.

[0021] Then, after removing 2Oaluminum3 substrate 1 by the dry etching by the ion beam of corrosive gas, along with the broken line C of drawing 3 (b) and drawing 4 (b), the ceramic-metal layered product 4 was cut for every component with the dicing saw. Ag paste was attached to the both ends of the ceramic-metal layered product 4 which it cut into one element at a time by dipping, it could be burned at 600 degrees C, and the external electrodes 5a and 5b were formed.

[0022] In this way, die length of about 1mm, 0.5mm of ****, and the stacked type ceramic condenser 6 with a thickness of about 0.45mm were obtained. When the capacity of this stacked type ceramic condenser 6 was measured, it was 1.1 micro F in value.

[0023] Using vacuum deposition as the formation approach of the example 2Pt layers 20a and 20b (conductor electrode 2a, 2b), other than this, it was alike, therefore die length of about 1mm, 0.5mm of ****, and the stacked type ceramic condenser 6 with a thickness of about 0.45mm were manufactured like the example 1. When the capacity of this stacked type ceramic condenser 6 was measured, the value of 1.0 micro F was acquired.

[0024] Die length of about 1mm, 0.5mm of ****, and the stacked type ceramic condenser 6 with a thickness of about 0.45mm were obtained like the example 1, using a spatter as the formation approach of the example 3Pt layers 20a and 20b (conductor electrode 2a, 2b). When the capacity of this stacked type ceramic condenser 6 was measured, the value of 1.1 micro F was acquired.

[0025]

[Effect of the Invention] Since according to this invention the precise film is obtained and neither a ceramic layer nor a conductor electrode is moreover put to an elevated temperature, even if it carries out lamination of a ceramic layer or the conductor electrode to 1 micrometer or less, it is hard to produce a defect in a ceramic layer or a conductor electrode, and highly efficient and micro laminating ceramic electronic parts can be obtained.

[0026] Moreover, if it is in this invention, since a ceramic layer ultra-thin as a base material and a conductor electrode can be grown up and the laminating of the substrate can be carried out by turns, laminating ceramic electronic parts can be manufactured to stability and homogeneity, and micro or super-thin laminating ceramic electronic parts can be manufactured by moreover removing a substrate finally.

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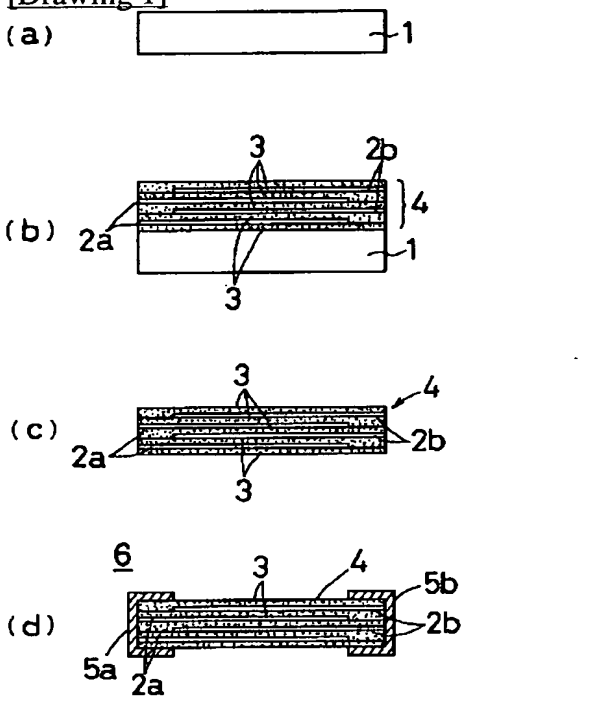
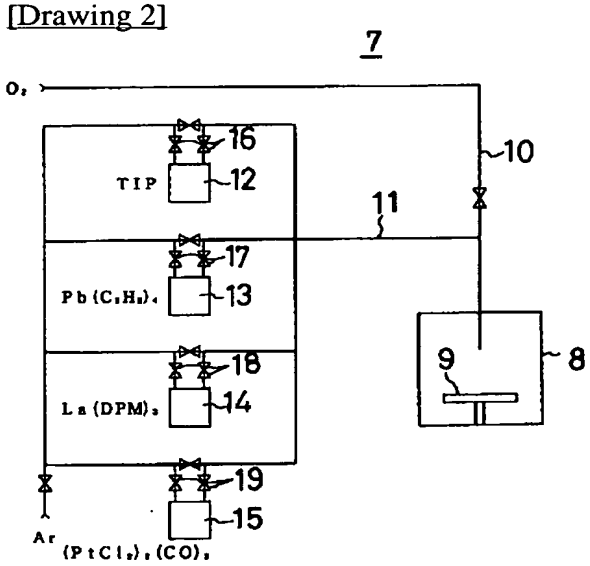
DRAWINGS

[Drawing 1]

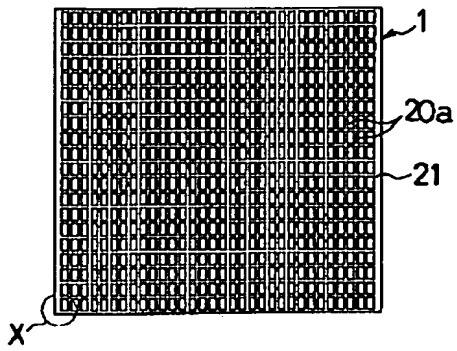


[Drawing 2]



[Drawing 3]

(a)



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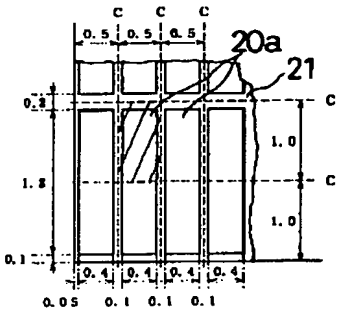
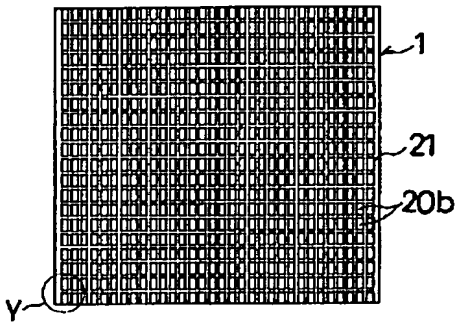


[Drawing 4]

(a)



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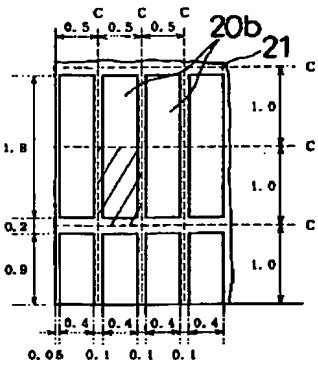

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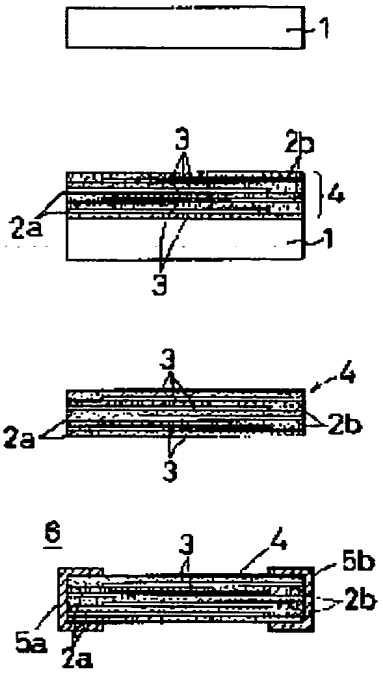

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[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平5－335173

(43)公開日　平成５年(1993)12月17日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｇ　4/12	３４６			
	３５２			
	３６４			

審査請求　未請求　請求項の数３(全　５　頁)

(21)出願番号　特願平4－164181

(22)出願日　平成４年(1992)５月28日

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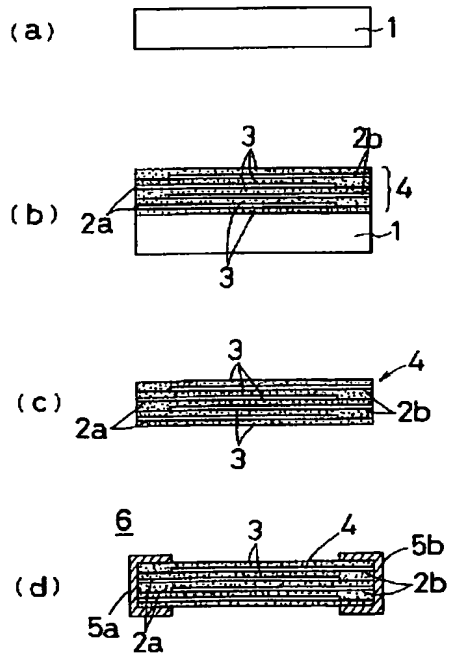
(54)【発明の名称】　積層セラミック電子部品及びその製造方法

(57)【要約】
【目的】　積層セラミック電子部品の高性能を実現しながら薄層化する。
【構成】　Al_2O_3基板１の上に、ＣＶＤ法、蒸着法もしくはスパッタ法による複数層の導電体電極２ａ，２ｂとＣＶＤ法による複数層のセラミック層３とからなるセラミック－金属積層体４を形成する。この後、Al_2O_3基板１をドライエッチング等によって選択的に除去し、セラミック－金属積層体４だけを残す。ついで、ディッピング等によって積層体４の両端に外部電極５ａ，５ｂを形成し、小型の積層セラミックコンデンサ６を得る。



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【特許請求の範囲】

【請求項１】　複数層の導電体電極と、ＣＶＤ法によって形成された複数層のセラミック層とを交互に積層したことを特徴とする積層セラミック電子部品。

【請求項２】　前記導電体電極をＣＶＤ法、蒸着法もしくはスパッタ法のうちの少なくとも１種の方法を用いて形成した請求項１に記載の積層セラミック電子部品。

【請求項３】　基板の上に導電体電極とＣＶＤ法によるセラミック層とを交互に複数層積層した後、前記基板を除去することを特徴とする積層セラミック電子部品の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は積層セラミック電子部品及びその製造方法に関する。具体的にいうと、ビデオテープレコーダ等の電子部品に広く用いられている積層セラミックコンデンサ、積層バリスタ、積層圧電素子、多層セラミック基板等の積層セラミック電子部品とその製造方法に関するものである。

【０００２】

【従来の技術】従来の積層セラミックコンデンサの製造方法を説明する（図示せず）。まず、素子寸法よりも大きな所定の大きさにカットされたセラミック生シート上に銀系ペースト等の電極ペースト（内部電極）を印刷し、乾燥させた後、この電極ペーストが印刷されたセラミック生シートを複数枚重ねて圧着させる。ついで、これを１素子の大きさにカットして焼成する。焼成後、内部電極と導通させるようにして素子の表面に電極ペーストを塗布し、これを焼き付けて素子の両端に外部電極を形成し、チップ状の積層セラミックコンデンサを製作している。

【０００３】

【発明が解決しようとする課題】近年、電子部品の分野においては、電子回路の高密度化・高集積化に伴って、積層セラミックコンデンサ等の電子部品の一層の微小化および高性能化が望まれている。したがって、積層セラミックコンデンサにおいて、容量を小さくすることなく微小化するためには、セラミック層（誘電体層）の厚みをできるだけ薄くすることが望まれる。

【０００４】しかしながら、従来のような積層セラミックコンデンサにおいてセラミック層の厚みを薄くしようとすると、種々の問題があった。まず、セラミック層を薄くするためには、セラミック原料粉末粒径を小さくする必要があるが、セラミック原料粉末の粒径の微小化には限度がある。また、セラミック層を薄くすると、内部電極の厚みも薄くする必要があるため、焼成工程において内部電極に電極切れが生じ易い。さらに、セラミック層を薄くすると、焼成時における内部電極の異常成長によりショートが発生したり、セラミック層に発生した孔によって耐圧が低下する等の問題が生じる。このため、

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従来の積層セラミックコンデンサにあっては、セラミック層の厚みを数μｍより薄くすることは不可能で、積層セラミックコンデンサの微小化及び大容量化には限界があった。

【０００５】本発明は叙上の従来例の欠点に鑑みてなされたものであり、その目的とするところは、積層セラミック電子部品の高性能を実現しながらセラミック層を薄層化することにある。

【０００６】

【課題を解決するための手段】本発明による積層セラミック電子部品は、複数層の導電体電極と、ＣＶＤ法によって形成された複数層のセラミック層とを交互に積層したことを特徴としている。

【０００７】さらに、上記導電体電極はＣＶＤ法、蒸着法もしくはスパッタ法のうちの少なくとも１種の方法を用いて形成することができる。

【０００８】また、本発明による積層セラミック電子部品の製造方法は、基板の上に導電体電極とＣＶＤ法によるセラミック層とを交互に複数層積層した後、前記基板を除去することを特徴としている。

【０００９】

【作用】本発明の積層セラミック電子部品にあっては、セラミック層がＣＶＤ法によって形成され、さらに、導電体電極がＣＶＤ法、蒸着法、スパッタ法等によって形成されているので、セラミック層及び導電体電極のいずれも緻密な膜が形成され、しかも、焼成等の加熱工程を経ないので、導電体電極の電極切れ、ショート等の欠陥が生じにくく、電子部品としての高性能化が可能となる。

【００１０】さらに、セラミック層がＣＶＤ法によって形成され、導電体電極がＣＶＤ法、蒸着法、スパッタ法等によって形成されているので、セラミック層や導電体電極の１μｍ以下の薄層化が可能となり、超小型の積層セラミック電子部品が得られる。

【００１１】また、本発明の積層セラミック電子部品の製造方法にあっては、基板の上にセラミック層及び導電体電極を形成しているので、基板を支持体として極薄のセラミック層及び導電体電極を成長させ、交互に積層させることができる。しかも、最終的には基板を除去しているので、基板によって積層セラミック電子部品が大きくなることがなく、上記のような超小型の積層セラミック電子部品を製作することができる。

【００１２】

【実施例】図１（ａ）（ｂ）（ｃ）（ｄ）は、本発明の一実施例による積層セラミックコンデンサの製造方法を示している。図１（ａ）に示すものは表面が平滑な基板１であって、エッチング等によって選択的に除去可能な材質であればよく、絶縁基板に限定されない。例えば、アルミナ基板等を用いることができる。この基板１の上には、図１（ｂ）に示すように、セラミック層３が形成

され、その上に１層目の導電体電極２ａが形成され、その上にセラミック層３が形成され、さらに２層目の導電体電極２ｂが形成され、さらにセラミック層３が形成され、その上に３層目の導電体電極２ａが形成される。このような工程を繰り返すことにより、基板１の表面には導電体電極２ａ，２ｂとセラミック層３とが交互に複数層ずつ積層され、複数層の導電体電極２ａ，２ｂと複数層のセラミック層３とからなるセラミック－金属積層体４が形成される。ここで、各セラミック層３はＣＶＤ法によって形成され、各導電体電極２ａ，２ｂはＣＶＤ法、蒸着法もしくはスパッタ法のうちいずれかの方法を用いて形成されており、各セラミック層３及び各導電体電極２ａ，２ｂの厚みは１μｍ以下としてある。また、内部電極となる導電体電極２ａ，２ｂはマスクを用いてパターン化されており、奇数層目の導電体電極２ａと偶数層目の導電体電極２ｂとは、交互に反対側の端部へ引き出されている。この後、基板１をエッチング等によって選択的に除去すると、図１（ｃ）に示すようなセラミック－金属積層体４だけが残る。ついで、ディッピングやスパッタ等によって両端に外部電極５ａ，５ｂを形成すると、奇数層目の導電体電極２ａが一方の外部電極５ａと導通し、偶数層目の導電体電極２ｂが他方の外部電極５ｂと導通し、図１（ｄ）に示すような超小型の積層セラミックコンデンサ６が製作される。

【００１３】なお、図１では１素子のみの製造工程について説明しているが、複数素子を同時に製作することにより効率的に積層セラミックコンデンサを製造することができる。

【００１４】つぎに、本発明をより明確に説明するため、以下に具体的実施例を掲げて説明する。

実施例１

図２は積層セラミックコンデンサ６の製作に用いた熱ＣＶＤ装置７の概略構成図であって、８はＣＶＤ用のチャンバー、９は基板１をセットするためのサセプタ、１０はO_2ガスの給送路、１１はＡｒキャリアガスの給送路、１２はＴＩＰ〔チタンイソプロポキシド〕のベッセル、１３は$Pb(C_2H_5)_4$のベッセル、１４はＬａ（ＤＰＭ）$_3$〔ＤＰＭ＝$C_{11}H_{19}O_2$〕のベッセル、１５は$(PtCl_2)_2(CO)_3$のベッセルであって、ＴＩＰ、$Pb(C_2H_5)_4$、Ｌａ（ＤＰＭ）$_3$及び$(PtCl_2)_2(CO)_3$の各ベッセル１２，１３，１４，１５はＡｒキャリアガスの給送路１１に並列に配置されている。

【００１５】積層セラミックコンデンサ６を製作するための基板１として縦横各５０ｍｍ、厚さ０．２ｍｍのAl_2O_3基板を用い、このAl_2O_3基板１を熱ＣＶＤ装置７のサセプタ９上にセットした。

【００１６】ついで、サセプタ９を６００℃に加熱した状態で、ＴＩＰ、$Pb(C_2H_5)_4$及びＬａ（ＤＰＭ）$_3$の各ベッセル１２，１３，１４の各バルブ１６，１７，１８を開き、気化したＴＩＰ、$Pb(C_2H_5)_4$及びＬａ（ＤＰＭ）$_3$の各原料ガスをＡｒキャリアガスに乗せてチャンバー８へ送り、この原料ガスをO_2ガスと共にAl_2O_3基板１に吹き付けて反応させ、厚さ約１μｍのＰＬＴ薄膜２１（セラミック層３）を形成した（以下、ＰＬＴ薄膜形成工程という）。

【００１７】次に、ＰＬＴ薄膜２１の上にメタルマスクをセットし、基板１を６００℃に加熱した状態で$(PtCl_2)_2(CO)_3$のベッセル１５のバルブ１９を開き、$(PtCl_2)_2(CO)_3$の原料ガスをＡｒキャリアガスと共にメタルマスクの窓を通してAl_2O_3基板１に吹き付け、図３（ａ）（ｂ）に示すようにメタルマスクの窓と同一パターンに厚さ約０．５μｍのＰｔ膜２０ａ（導電体電極２ａ）を形成した（以下、Ｐｔ膜形成第１工程という）。図３（ｂ）は図３（ａ）のＸ部拡大図であって、斜線を施した領域は１素子分に相当する領域を示し、図３（ｂ）に記入されている数字は各部の寸法（単位ｍｍ）を示している。

【００１８】ついで、再びＰＬＴ薄膜形成工程によりＰＬＴ薄膜２１を約１μｍ生成させた。

【００１９】次に、最上層のＰＬＴ薄膜２１の上に別なメタルマスクをセットし、基板１を６００℃に加熱した状態で$(PtCl_2)_2(CO)_3$のチャンバー１５のバルブ１９を開き、$(PtCl_2)_2(CO)_3$の原料ガスをＡｒキャリアガスと共にメタルマスクの窓を通してAl_2O_3基板１に吹き付け、図４（ａ）（ｂ）に示すようにメタルマスクの窓と同一パターンに厚さ約０．５μｍのＰｔ膜２０ｂ（導電体電極２ｂ）を形成した（以下、Ｐｔ膜形成第２工程という）。図４（ｂ）は図４（ａ）のＹ部拡大図であって、斜線を施した領域は１素子分に相当する領域を示し、図３（ｂ）に記入されている数字は寸法（単位ｍｍ）を示している。

【００２０】このように、ＰＬＴ薄膜形成－Ｐｔ膜形成第１－ＰＬＴ薄膜形成－Ｐｔ膜形成第２の各工程を１５０回繰り返し、最後にＰＬＴ薄膜形成工程を行なってAl_2O_3基板１の上にセラミック－金属積層体４を得た。

【００２１】この後、腐食性ガスのイオンビームによるドライエッチングでAl_2O_3基板１を除去した後、図３（ｂ）及び図４（ｂ）の破線Ｃに沿ってダイシングソーによりセラミック－金属積層体４を素子毎にカットした。１素子ずつにカットしたセラミック－金属積層体４の両端にディッピングによりＡｇペーストを付け、６００℃で焼き付けて外部電極５ａ，５ｂを形成した。

【００２２】こうして長さ約１ｍｍ、幅約０．５ｍｍ、厚さ約０．４５ｍｍの積層セラミックコンデンサ６を得た。この積層セラミックコンデンサ６の容量を測定したところ１．１μＦの値であった。

【００２３】実施例２

Ｐｔ層２０ａ，２０ｂ（導電体電極２ａ，２ｂ）の形成方法として蒸着法を用い、それ以外については実施例１

と同様にして長さ約1mm、幅約0.5mm、厚さ約0.45mmの積層セラミックコンデンサ6を製作した。この積層セラミックコンデンサ6の容量を測定したところ1.0μFの値が得られた。

【0024】実施例3

Pt層20a，20b（導電体電極2a，2b）の形成方法としてスパッタ法を用い、実施例1と同様にして長さ約1mm、幅約0.5mm、厚さ約0.45mmの積層セラミックコンデンサ6を得た。この積層セラミックコンデンサ6の容量を測定したところ1.1μFの値が得られた。

【0025】

【発明の効果】本発明によれば、セラミック層及び導電体電極のいずれも緻密な膜が得られ、しかも高温に曝されないので、セラミック層や導電体電極を1μm以下に薄層化してもセラミック層や導電体電極に欠陥が生じにくく、高性能で超小型の積層セラミック電子部品を得られる。

【0026】また、本発明にあっては、基板を支持体として極薄のセラミック層及び導電体電極を成長させ、交互に積層させることができるので、安定かつ均一に積層＊＊セラミック電子部品を製作でき、しかも、最終的には基板を除去することによって超小型もしくは超薄型の積層セラミック電子部品を製作することができる。

【図面の簡単な説明】

【図1】（a）（b）（c）（d）は本発明の一実施例による積層セラミックコンデンサの製造方法を示す断面図である。

【図2】本発明の具体的実施例において用いたCVD装置を示す概略構成図である。

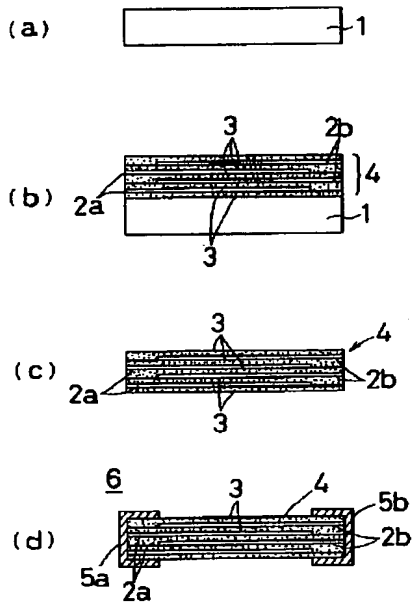
【図3】（a）は基板の上に形成されたPt膜（導電体電極）を示す平面図、（b）は（a）のX部拡大図である。

【図4】（a）は基板の上に形成された別なPt膜（導電体電極）を示す平面図、（b）は（a）のY部拡大図である。

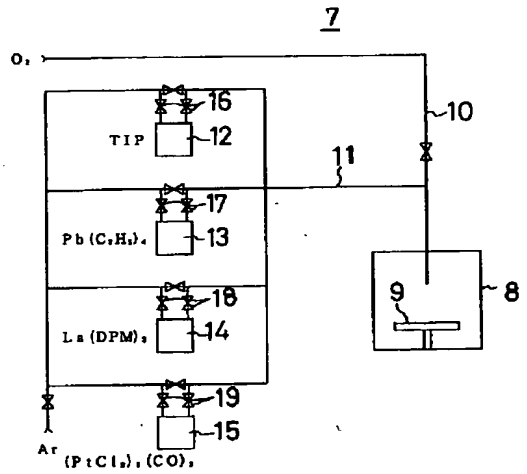
【符号の説明】

1　基板
2a，2b　導電体電極
3　セラミック層
5a，5b　外部電極
7　熱CVD装置

【図1】

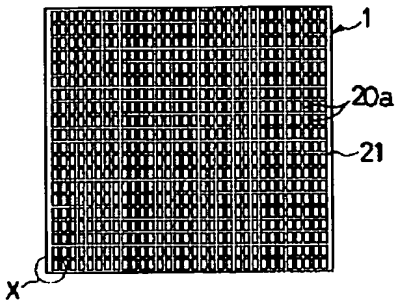


【図2】

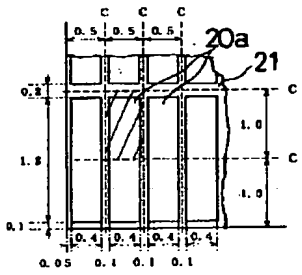


【図3】

(a)

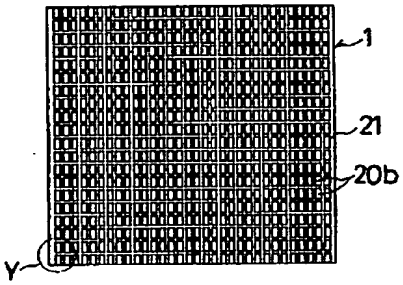


(b)



【図4】

(a)



(b)